**The Evolution of Computer Systems**

Joseph Baskin

CMSC310 – Computer Systems and Architecture

Professor Jack Lusby

The current generation of humans alive has seen amazing advancements in technology and in computer systems of the past. At the turn of the century, typical computers of the era utilized simple single-core CPUs with minimal cache memory and further limited system memory. Fast-forward to today, low end computers more than quadruple the capacity and performance of those earlier computers. These early computers utilized Reduced Instruction Set Computing (RISC) cores and, in some cases, today, RISC processors are used for various reasons. RISC instruction sets, and their evolution over the last 25 years, are likely the greatest enhancement to modern-day computing.

To understand the magnitude of advancement that our modern computers have, there is a minimum level of knowledge about early computers that should be understood. In 1998, AMD released the K6 -series processors, which utilized a single-core, single-clock with a rate ranging from 200 MHz up to 570 MHz and used a microprocessor that converted 6 instruction sets per clock from x86 (Complex Instruction Set Computing, CISC) issues to RISC using a microarchitecture titled RISC86. This processor also used a 64 Kbyte L1 cache, considered large for its time. (DOS Days, n.d.)

In comparison, the Intel 12th Generation i5-600 series CPUs use 10 cores with a clock speed ranging from 2.8 GHz up to 4.9 GHz. The processing units run on the x86 CISC architecture and contain a 20 Mbyte cache broken up over L1 and L2 series memories. (Intel, 2023) This processor contains a minimum of 14 times the speed of the AMD K6-2 processor, an extraordinary increase in that time frame.

Another good comparison to look at is Apple’s M1 chipset utilizes an 8-core design with a clock speed of 3.2 GHz and has different cached memory for the performance (12 Mbytes of shared L2 Cache) and the efficiency (4 Mbytes of shared L2 Cache) cores. Apple, however, decided to use the Advanced RISC Machine (ARM) base for their chipsets across all their platforms, including the M1 chipset. Because of the design of RISC processor units, their high efficiency and simple instructions make the processors perform better than similarly classed x86 processors, increasing their function in pipelining instructions.

With the increase in RISC and CISC computing, came the development of pipelining instructions, where one set of instructions are overlapping in queue with another set of instructions from the control unit. This enables CPUs to execute instruction sets faster than in a non-pipelined architecture (Nikolic et al, 2022). While pipelining was integral to early computing systems, modern CPUs with multiple cores can use a variety of techniques to accomplish what pipelining did previously.

Like the number of cores and efficiency advances in technology and design brought to CPUs chipsets, it brought equal advances in the cache memory, located on the chipset die. Notably, the Level 1 cache has been split into Instruction cache (I-cache) and a data cache (D-cache) (Jacob, et al, 2008). The instruction cache is responsible for storing commonly executed instruction sets that the control unit would utilize in processing input and outputs.

The early AMD K6-2 processor used a single 32 Kbyte instruction cache, significantly limiting the CPU’s ability to execute large instruction sets quickly (DOS Days, n.d.). Today’s modern processors use the same cache set up (I- and D- caches), however, each core has its own associated I-cache. In the i5 processor, the chipset employs 6, 32 Kbyte and 4, 64 Kbyte I-Caches to store instructions (Intel, 2023), and the Apple M1 chipset employs 4, 48 Kbyte and 4, 32 Kbyte I-caches to store instruction (Wikimedia Foundation, 2024).

The size of the cache memory associated with the chipset becomes important when compared to the computing type. Many people laud Apple computers for their speed and performance in processing images, videos, and other multimedia, due to the Advanced RISC computing employed in the chipset. Enhancements in the RISC instruction set architecture have led to faster and faster processing times when compared to the x86 processors, even in modern computing. While a normal user may not be able to notice and/or clock the difference between an ARM equipped computer versus an x86 equipped computer, as instruction sets are retrieved, queued for, and executed, the time it takes may become exponential, from boot time to being able to start using the computer. RISC-based computers, regardless of actual clock speed, have shown to be more efficient and faster than their CISC counterparts.

IBM first utilized the RISC instruction sets in the telephone-switching machine dubbed “the 801” (Cocke, 2000). In modern computing systems, RISC and CISC systems are typically hybrids, in that, many of the overhead instructions are executed using the CISC instruction set architecture and the rest of the instructions are executed using RISC instruction set architecture.

Over the last 25 years, computing technology has evolved from single-core low-speed processors with low amounts of instruction cache memory to complex systems with multiple cores of differing types, high speed processing units, and large per core cache memory allocations. RISC has played a the most significant role in helping advance this technology, through keeping instruction sets simple for quick execution, low emission, and low energy absorption. It will be very interesting to see the continued development of computer systems as Artificial Intelligence and Quantum computing become more prevalent.

**References**

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